UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/757,249	01/14/2004	Jimmie Earl DeWitt JR.	AUS920030554US1	6477

35525 7590 02/28/2006

IBM CORP (YA)
C/O YEE & ASSOCIATES PC
P.O. BOX 802333
DALLAS, TX 75380

EXAMINER	
SAVLA, ARPAN P	

ART UNIT	PAPER NUMBER
2185	

DATE MAILED: 02/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/757,249	DEWITT ET AL.	
	Examiner	Art Unit	
	Arpan P. Savla	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *2-7,9-14 and 16-21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/14/04, 7/1/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. 10/757,249 has a total of 21 claims pending in the application, there are 3 independent claims and 18 dependent claims, all of which are ready for examination by Examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

1. Applicant's oath/declaration has been reviewed by Examiner and is found to conform to the requirements prescribed in 37 CFR 1.63.

INFORMATION CONCERNING DRAWINGS

Drawings

2. Applicant's drawings submitted January 14, 2004 are acceptable for examination purposes.

ACKNOWLEDGMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

3. As required by MPEP § 609(c), Applicant's submission of both Information Disclosure Statements dated January 14, 2004 and July 1, 2005 are acknowledged by Examiner and cited references have been considered in the examination of the claims now pending. As required by MPEP § 609 c(2), a copy of the PTOL-1449 initialed and dated by Examiner is attached to the instant office action.

OBJECTIONS

Specification

4. The disclosure is objected to because of the following informalities:

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

6. In the section entitled "Cross Reference to Related Applications" Applicant must properly identify all co-pending applications with their corresponding application numbers (i.e. serial numbers).

Appropriate correction is required.

REJECTIONS NOT BASED ON PRIOR ART

Claim Rejections - 35 USC § 101

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. **Claims 8-14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.** Claims 8-14 are not limited to tangible embodiments. In view of Applicant's disclosure, pg. 125, line 23 – pg. 126, line 11, the computer readable medium is not limited to tangible embodiments, instead being define as including both tangible embodiments (e.g. recordable-type media, such as a floppy disk, hard disk drive, a RAM, CD-ROMS, and DVD-ROMS) and intangible embodiments

(e.g. transmission forms, such as radio frequency and light wave transmissions). As such, claims 8-14 are not limited to statutory subject matter and are therefore non-statutory.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 2-7, 9-14, and 16-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

11. **As per claims 2, 3, 7, 9, 10, 14, 16, 17, and 21**, the claims recite the limitation "the reload operation" in lines 7, 1, 3, 9, 2, 4, 7, 2, and 3 respectively. There is insufficient antecedent basis for this limitation in the claims. Applicant may consider amending the claims to read "the reload."

12. **Claims 3-6, 10-13, and 17-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.**

13. **As per claims 3, 4, 10, 11, 17, and 18**, it is unclear whether the "value of the first processor access flag bit" recited in lines 11, 7, 13, 9, 12, and 8 respectively is the same as the "first value of the first processor access flag bit" recited in lines 4, 2, 5, 3, 4, and 2 respectively or a completely different "value of the first processor access flag bit."

Applicant may consider amending "first value of the first processor access flag bit" to read "value of the first processor access flag bit" instead.

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

14. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

15. Claims 1 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Gupta et al. (U.S. Patent 5,710,881).

16. **As per claim 1**, Gupta discloses a method, in a multiprocessor data processing system, for identifying false sharing of a cache line, comprising:

associating a performance indicator with at least one portion of a cache line in a cache (col. 11, lines 11-14; Fig. 4, elements 118 and 178); It should be noted that "data block" is analogous to "cache line." It should also be noted that when taking the broadest interpretation of the claim language it is clear that the limitations of the claim do not identify what "performance indicator" specifically entails. Gupta discloses a count for each data block, thus disclosing a "performance indicator."

providing a plurality of processor access flag bits for the at least one portion of the cache line in the cache, wherein there is at least one processor access flag bit for each processor of a plurality of processors in the multiprocessor data processing

system (col. 10, lines 57-59; col. 11, lines 31-34; Fig. 4, element 160); It should be noted that "suspend flag" is analogous to "processor access flag bit." It should also be noted that each processor can perform a suspend request, therefore, there is a suspend flag for each the processors in the system.

and responsive to an access operation to the at least one portion of the cache line, setting a processor access flag bit corresponding to a processor from which the access operation was received (col. 11, lines 36-50).

17. **As per claim 15**, Gupta discloses an apparatus, in a multiprocessor data processing system, for identifying false sharing of a cache line, comprising:

means for associating a performance indicator with at least one portion of a cache line in a cache (col. 11, lines 11-14; Fig. 4, elements 118 and 178); It should be noted that pg. 20, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, see citation note in the 102(b) rejection for claim 1 above.

means for providing a plurality of processor access flag bits for the at least one portion of the cache line in the cache, wherein there is at least one processor access flag bit for each processor of a plurality of processors in the multiprocessor data processing system (col. 10, lines 57-59; col. 11, lines 31-34; Fig. 4, element 160); It should be noted that pg. 20, lines 4-6 of Applicant's specification appear to define this means as a computer. Also, see citation note in the 102(b) rejection for claim 1 above.

and means for responsive to an access operation to the at least one portion of the cache line, setting a processor access flag bit corresponding to a processor from

which the access operation was received (col. 11, lines 36-50). It should be noted that pg. 20, lines 4-6 of Applicant's specification appear to define this means as a computer.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claim 8 is rejected under 35 U.S.C. 103(a) as being obvious over Gupta in view of Andrew S. Tanenbaum, "Structured Computer Organization, 2nd Edition," hereafter "Tanenbaum."

20. Gupta discloses associating a performance indicator with at least one portion of a cache line in a cache (col. 11, lines 11-14; Fig. 4, elements 118 and 178); See citation note in the 102(b) rejection for claim 1 above.

providing a plurality of processor access flag bits for the at least one portion of the cache line in the cache, wherein there is at least one processor access flag bit for each processor of a plurality of processors in the multiprocessor data processing system (col. 10, lines 57-59; col. 11, lines 31-34; Fig. 4, element 160); See citation note in the 102(b) rejection for claim 1 above.

and responsive to an access operation to the at least one portion of the cache line, setting a processor access flag bit corresponding to a processor from which the access operation was received (col. 11, lines 36-50).

Gupta does not expressly disclose a computer program product in a computer readable medium for identifying false sharing of a cache line, comprising:

first instructions for associating a performance indicator with at least one portion of a cache line in a cache;

second instructions for providing a plurality of processor access flag bits for the at least one portion of the cache line in the cache, wherein there is at least one processor access flag bit for each processor of a plurality of processors in a multiprocessor data processing system;

and third instructions for responsive to an access operation to the at least one portion of the cache line, setting a processor access flag bit corresponding to a processor from which the access operation was received.

Tanenbaum discloses that hardware and software are logically equivalent (pg. 11, line 11).

Gupta and Tanenbaum are analogous art because they are from the same field of endeavor, that being computer hardware.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to follow Tanenbaum's argument and implement Gupta's data merging apparatus using instructions on a computer program product in a computer-readable medium having (i.e. implement hardware using software).

The motivation for doing so would have been to optimize such factors as cost, speed, and reliability (Tanenbaum, pg. 11, lines 14-15).

Therefore, it would have been obvious to combine Gupta and Tanenbaum for the benefit of obtaining the invention as specified in claim 8.

Conclusion

STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by MPEP 707.70(i):

Allowable Subject Matter

21. **Claims 2-7, 9-14, and 16-21** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims

22. **Claims 9-14** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 101 set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

23. **Claims 2-7, 9-14, and 16-21** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

24. The primary reasons for allowance of **claims 2-7, 9-14, and 16-21** in the instant application is the combination with the inclusion in these claims that "**determining if the reload operation is due to false sharing of the cache line based on the values of the processor access flag bits for each portion of the cache line.**" The prior art of record neither anticipates nor renders obvious the above recited combination.

25. If the applicant should choose to rewrite the independent claims to include the limitations recited in either one of **claims 2-7, 9-14, and 16-21**, Applicant is encouraged to amend the title of the invention such that it is descriptive of the invention as claimed as required by sec. 606.01 of the MPEP. Furthermore, the Summary of the Invention and the Abstract should be amended to bring them into harmony with the allowed claims as required by paragraph 2 of sec. 1302.01 of the MPEP.

26. As allowable subject matter has been indicated, Applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

RELEVANT ART CITED BY THE EXAMINER

The following prior art made of record and not relied upon is cited to establish the level of skill in Applicant's art and those arts considered reasonably pertinent to Applicant's disclosure. See MPEP 707.05(e).

1. U.S. Patent 5,710,881 discloses a data merging method and apparatus for shared memory multiprocessing computer systems.

2. U.S. Patent 5,822,763 discloses cache coherence protocol for reducing the effects of false sharing in non-bus-based shared-memory multiprocessors.

3. U.S. Patent 5,928,334 discloses a method for detecting synchronization violations in a multiprocessor computer system.

4. U.S. Patent 6,094,709 discloses a method of reducing false sharing in a shared memory system by enabling two caches to modify the same line at the same time.

5. U.S. Patent 6,285,974 discloses a method for detecting architectural violations in a multiprocessor computer system.

6. U.S. Patent 6,636,950 discloses computer architecture for shared memory access.

7. U.S. Patent Application Publication 2004/0205302 discloses a method and system for postmortem identification of falsely shared objects.

Non-Patent Literature

Torrellas et al., "False Sharing and Spatial Locality in Multiprocessor Caches", June 1994, IEEE Transactions on Computers, Vol. 43, No. 6, pp. 651-663.

Rothman et al., "Analysis of Shared Memory Misses and Reference Patterns", 2000, IEEE, pp. 187-198.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Arpan P. Savla whose telephone number is (571) 272-1077. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Arpan Savla
Assistant Examiner
Art Unit 2185
February 16, 2006

DONALD SPARKS
SUPERVISORY PATENT EXAMINER